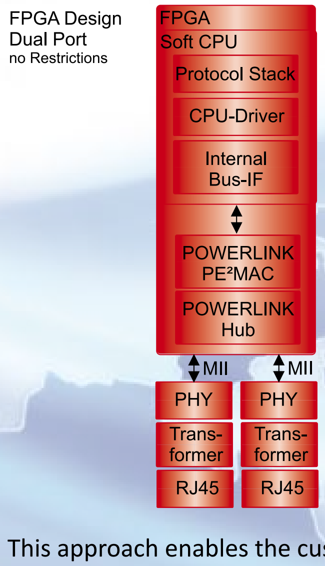
POWERLINK - Use Cases

ETHERNET POWERLINK

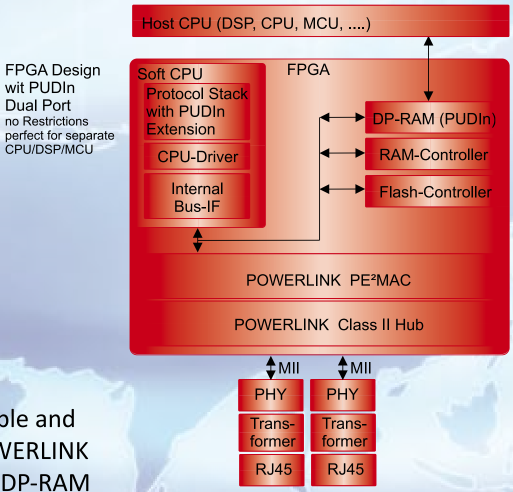
port PROFESSIONAL INDUSTRIAL COMMUNICATION

POWERLINK – Use Cases in open, POWERLINK compatible networks

POWERLINK with FPGA and Soft-CPU
This case is the most common use case, it allows for an excellent POWERLINK Performance and supports all outstanding POWERLINK features.
In this scenario a Hub-IP Core ensures low latency and low jitter in the line-structure of the network.
A special component PE²MAC (POWERLINK Enhanced Ethernet MAC) provides a Autoreply functionality, which basically answers Poll-Request from the MN almost instantly with the corresponding Poll-Response. This results in an overall excellent performance and specially low jitter.
In a Soft-CPU in the same FPGA the POWERLINK Protocol is being managed and the customer's application is running.



As a further improvement a DP-RAM can be employed – so the customer's sensible application runs in a additional, external CPU and the Soft-CPU only manages the POWERLINK Protocol.



This approach enables the customer to run his complex, sensible and often already existing design almost unchanged while the POWERLINK objects are accessed as an external memory, that s located as DP-RAM in the FPGA.

Available Products from port:
Protocol Stack (with PUDIn Support)
POWERLINK CN Protocol Stack, ANSI-C Source Code
Driver for MCU (NIOS or Microblaze)
For POWERLINK CN Protcolo Stack, ANSI-C Source Code
POWERLINK DesignTool
Tool for generating fast and costeffective POWERLINK applications (Controlled Nodes).
POWERLINK-Hub IP-Core
POWERLINK HUB IP - Core for XILINX or Altera FPGA, VHDL Source Code. The EPL Hub is optimized for low latency.
POWERLINK MAC (PE²MAC)
POWERLINK Enhanced Ethernet MAC IP-Core, VHDL Source Code für Xilinx or Altera FPGAs. The MAC offers extremely fast Poll Responses operating POWERLINK.

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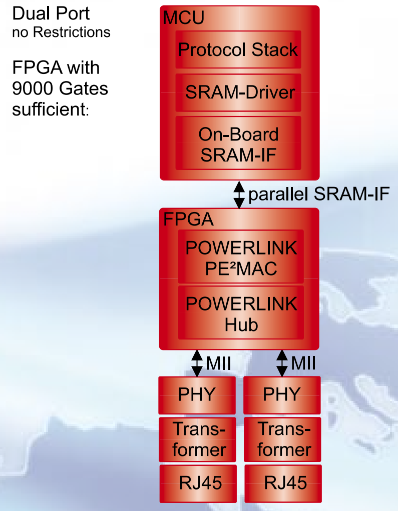
POWERLINK with FPGA and external MCU

This use case allows to combine the advantages of high speed / low jitter connectivity of the FPGA Ethernet access solution with the performance and the perherial components of a silicon MCU.

Existing or price effective silicon MCUs with Flash/RAM and the proper peripherials on-board are often good enough for reasonable POWERLINK performance.
They add less money and components to the BOM than the external SD-RAM and serial Flash for the Soft-CPU would add.
Depending on the Software-Design and the System-Load Cycle Times down to 1ms can be realised.



Available Products from port:

Protocol Stack
POWERLINK CN Protocol Stack, ANSI-C Source Code
Driver for MCU (STM32, Luminary, ...)
For POWERLINK CN Protcolo Stack, ANSI-C Source Code
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POWERLINK with FPGA and external Linux-CPU

Instead of the MCU a powerfull CPU (e.g. Arm9, i.MX) can be employed.

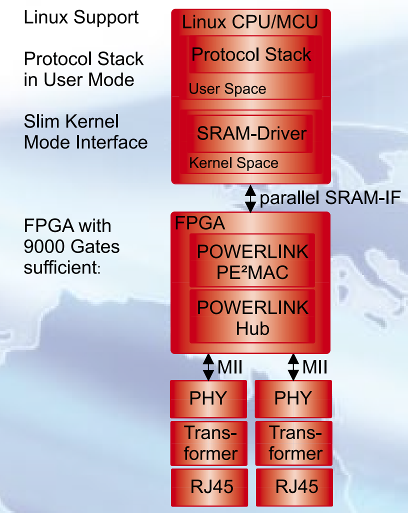
Normally running POWERLINK on Linux Systems would limit cycle time and possible jitter to values that are not acceptable for industrial applications.

Combining the Linux CPU with the FPGA enables the Linux CPU at least theoretical to manage all possible cycle times and low jitter. The bottleneck is now the protocol stack that would need to run completely in the Kernel Space in Kernel-Mode to comply to POWERLINK's speed requirements.

Bringing large protocol libraries into the Kernel-Mode increases risks and reduces overall stability of the Linux system.

Therefore port has created a Kernel-Mode POWERLINK Kernel Mode Interface that runs in the Kernel Space while ports POWERLINK Library runs in the User-Mode.

This separation enables Linux for the industrial grade cycle times and jitter AND maintains the Linux concept of a fast Kernel-Mode Interface and a dedicated User-Mode application.



Linux Support

Protocol Stack in User Mode

Slim Kernel Mode Interface

FPGA with 9000 Gates sufficient:

Linux CPU/MCU

Protocol Stack

User Space

SRAM-Driver

Kernel Space

parallel SRAM-IF

FPGA

POWERLINK PE²MAC

POWERLINK Hub

MII

MII

PHY

PHY

Trans-former

Trans-former

RJ45

RJ45

Available Products from port:

Protocol Stack

POWERLINK CN Protocol Stack, ANSI-C Source Code

Driver for CPU (GPL Kernel Mode Interface)

For POWERLINK CN Protcolo Stack, ANSI-C Source Code

POWERLINK DesignTool

Tool for generating fast and costeffective POWERLINK applications (Controlled Nodes).

POWERLINK-Hub IP-Core

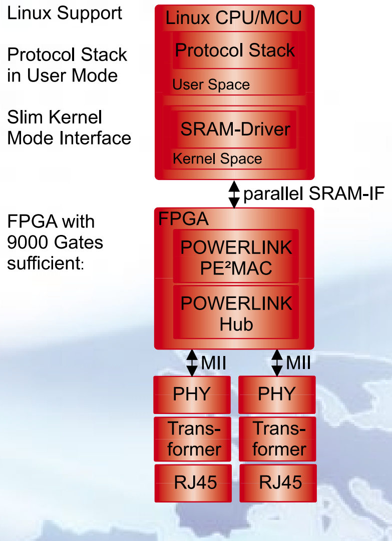
POWERLINK HUB IP - Core for XILINX or Altera FPGA, VHDL Source Code. The EPL Hub is optimized for low latency.

POWERLINK MAC (PE²MAC)

POWERLINK Enhanced Ethernet MAC IP-Core, VHDL Source Code für Xilinx or Altera FPGAs. The MAC offers extremely fast Poll Responses operating POWERLINK.

POWERLINK with Linux SoC

A special use-case of the Linux System is the SoC (e.g. ZYNQ)
Here the FPGA and a powerful Linux CPU are combined on a single chip.
Here as well the advantages of the Kernel-Mode Interface and the User Mode operated POWERLINK protocol stack are combined.
Linux becomes enabled for the industrial grade cycle times and jitter AND Linux' concept of a fast Kernel-Mode Interface and a dedicated User-Mode application is maintained.



Available Products from port:

Protocol Stack
POWERLINK CN Protocol Stack, ANSI-C Source Code
Driver for ZYNQ (GPL Kernel Mode Interface)
For POWERLINK CN Protcolo Stack, ANSI-C Source Code
POWERLINK DesignTool
Tool for generating fast and costeffective POWERLINK applications (Controlled Nodes).
POWERLINK-Hub IP-Core
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POWERLINK - Use Cases

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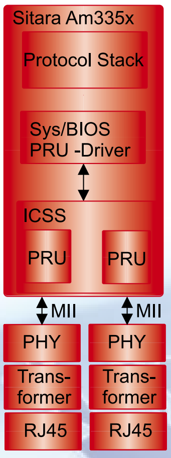
POWERLINK with TI's Sitara AM335x
Port's POWERLINK Protocol Library supports POWERLINK on TI's versatile platform Sitara.
The on-chip periphrials ICSS (Industrial Communication Sub System) with the parts PRU (Programmanle Real Time Units) deliver an outstanding support for the POWERLINK specific support in ()programmable) hardware.
Besides POWERLINK other Ethernet based fieldbusses are supported as well.
Currently TI's Real Time OS Sys/BIOS is supported, Linux Support is under construction.

POWERLINK on TI's PRUs

- excellent POWERLINK Performance

- integrated POWERLINK periphrials



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Protocol Stack
POWERLINK CN Protocol Stack, ANSI-C Source Code
Driver for Sitara (AM335x)
For POWERLINK CN Protcolo Stack, ANSI-C Source Code
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POWERLINK - Use Cases

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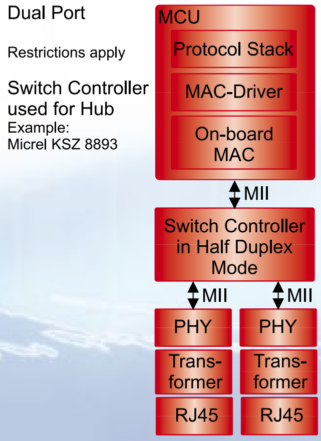
The following Use Cases are only suitable for applications with limited POWERLINK requirements. Significant limitations in Cycle Time, Jitter and Latency apply.

POWERLINK with Repeater-Mode Switch Controller and external CPU
This approach combines the price effective silicon MCUs with Flash/RAM and the proper peripherials on-board with a Silicon Switch controller for provinding line structure.
Some Switch controller manufacturer provide a feature calle Repeater Mode, which provides lowlatency and low jitter troughout the network.
This approach – providing Line Structure – comes with the lowest BOM cost, however shorther cycle times than 1ms are not possible.



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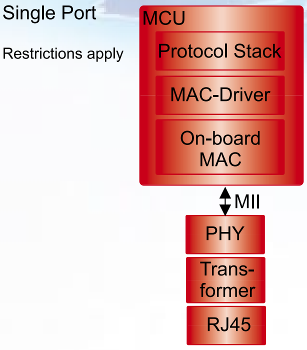
POWERLINK with CPU in Star Structure
This use case describes the lowest cost BOM approach – utilizing the start structure topology. The POWERLINK Protocol Stack is employed on the same MCU as the application is running. This makes sense for cost sensitive applications with only medium performance requirements. A cycle time down to 1ms is possible – however this depends on the software architecture.



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POWERLINK - Use Cases

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POWERLINK – available components and Tools by port

Protocol Stack = Library + Driver

The POWERLINK Protocol Stack for Controlled Nodes (CNs) by port provides POWERLINK functionality for devices.
The Protocol Stack consists from the POWERLINK Library and the POWERLINK Driver. While the Library is hardware independent, the Driver connects the Library to the specific hardware and optional to the OS.
This way the Library can be used on almost any hardware platform without "porting" it to the new hardware platform. Only the Driver needs to be created with significantly less effort. The POWERLINK Protocol Stack can be used with Operating Systems (OS) and without – running on plain hardware.
Several hardware platforms are currently supported: STR9, STM32, Luminary, Am335x, NIOS and MicroBlaze.
The Kernel-Mode Linux Driver for port's POWERLINK enables Linux POWERLINK applications for the high POWERLINK performance of the Kernel-Mode solution but maintains the integrity of the system with the Library running in User-Mode.
While the MCU platforms (STM32, Luminary) are able to provide cost effective, low ressource POWERLINK connectivity, the FPGA solutions enables Embedded Systems for the maximum POWERLINK performance.

Advantages/USPs

- FPGAs supported as well as MCUs and Linux Systems
- Suitable for Embedded Systems with no or any OS
- Suitable for high performance Linux applications
  - o Kernel-Mode Driver
  - o User-Mode Library
- New platforms easy supported
- DesignTool support
- Delivery in Source Code

POWERLINK MAC (PE^{2}MAC)

Port's POWERLINK Enhanced Ethernet MAC (PE^{2}MAC) is a VHDL written IP-Core for Altera and Xilinx FPGAs.
The Core of the PE^{2}MAC is a set of Compare/Capture Registers that can trigger on the Poll-Request message, sent by the Managing Node (MN). Upon reception of the Poll-Request message the PE^{2}MAC automatically responds "in hardware" with the preconfigured Poll-Response message. This functionaltity enables the CN for cycle times down to 200µs and for an exceptional low jitter over the complete network.
The PE^{2}MAC operates best with port's POWERLINK Hub and port's POWERLINK Protocol Stack.

POWERLINK Hub

The POWERLINK Hub by port is a Class 2 Repeating Hub wit 3 MII-ports for use in POWERLINk networks. It only introduces below 360ns delay (including delay by the PHYs) and less than 40ns Jitter.
The POWERLINK Hub integrates seamless with the PE^{2}MAC
Missing Driver or missing Feature
Port is available for creating new driver or missing features.

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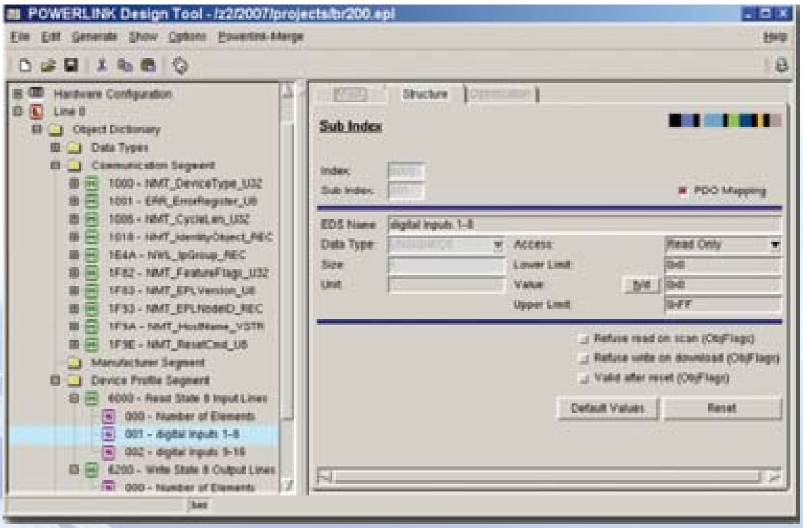
DesignTool

Port's POWERLINK DesignTool configures the Library, the Driver, the Objects and creates the XDD-File.

Port's POWERLINK DesignTool generates the 'fabric' to combine User-Application, Protocol-Stack and the XDD-File to be a POWERLINK CN-Device.

The SW-Engineer configures using this GUI-Tool port's POWERLINK Protocol Stack, creates the POWERLINK-objects and creates his own variables-definitions. Upon pressing a button the tool creates the 'fabric', consisting from various Header-Files and from the XDD-File. Further a reasonable documentation is created.

The DesignTool saves development time, reduces design cycles and improves the quality of the product creation process.


POWERLINK Design Tool - /z2/2007/projects/br200.epl
File Edit Generate Show Options Powerlink-Merge Help
Structure
Optimization
Default Values
Reset

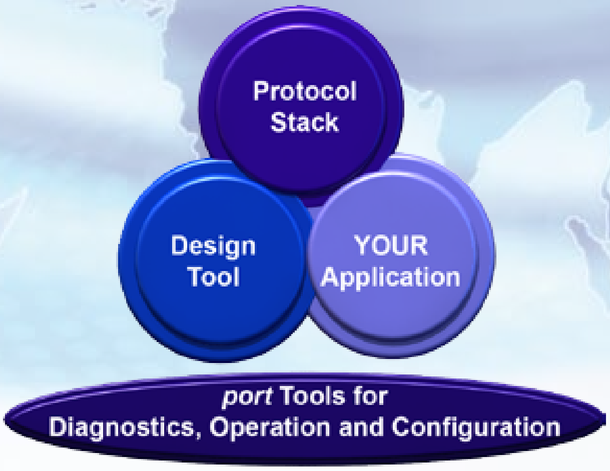
Hardware Configuration
Line 0
Object Dictionary
Data Types
Communication Segment
1000 - NMT_DeviceType_U32
1001 - ERR_ErrorRegister_U8
1006 - NMT_CycleLen_U32
1018 - NMT_IdentityObject_REC
1E4A - NWL_IpGroup_REC
1F82 - NMT_FeatureFlags_U32
1F83 - NMT_EPLVersion_U8
1F93 - NMT_EPLNodeID_REC
1F9A - NMT_HostName_VSTR
1F9E - NMT_ResetCmd_U8
Manufacturer Segment
Device Profile Segment
6000 - Read State 8 Input Lines
000 - Number of Elements
001 - digital inputs 1-8
002 - digital inputs 9-16
6200 - Write State 8 Output Lines
000 - Number of Elements

Sub Index

Index:
Sub Index:
● PDO Mapping

EDS Name: digital inputs 1-8
Data Type:
Access: Read Only
Size:
Lower Limit: 0x0
Unit:
Value: 0x0
Upper Limit: 0xFF

□ Refuse read on scan (ObjFlags)
□ Refuse write on download (ObjFlags)
□ Valid after reset (ObjFlags)



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